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ABSTRACT

The ASCII (American Standard Code for Information Interchange) decoder described here accepts inputs from an acoustic coupler, or Modem, in a remote time-sharing system. On receipt of a special command character the decoder recognizes, stores, and decodes the next two decimal digits. The output can be used to access any one of 100 items. For example, the decoder allows a random-access slide projector to be operated under computer control. The report contains complete specifications, including a description of the functions of the circuits in the decoder. (Author)

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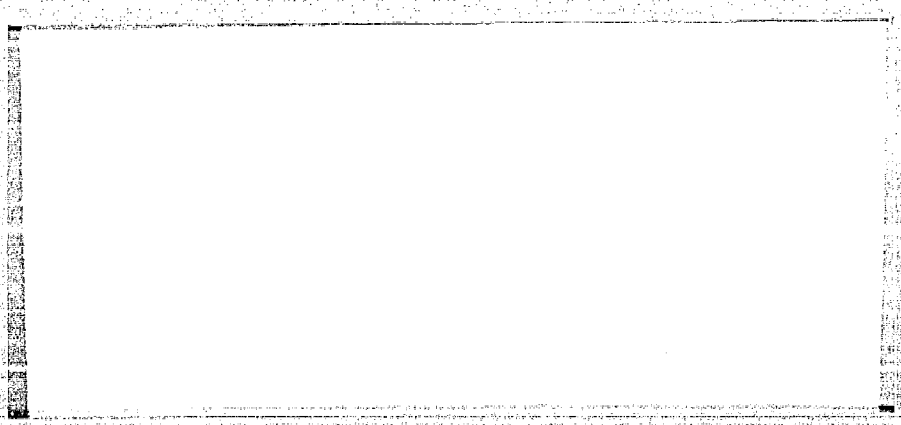

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A GENERAL-PURPOSE ASCII DECODER FOR CONTROL OF PERIPHERAL DEVICES FOR CAI TERMINALS

January 1972

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The ASCII decoder described in this report accepts inputs from an acoustic coupler, or Modem, in a remote time-sharing system. On receipt of a special command character the decoder recognizes, stores and decodes the next two decimal digits. The output can be used to access any one of 100 items. For example, the decoder allows a random-access slide projector to be operated under computer control.

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SECTION I. REQUIREMENT FOR AN ASCII DECODER

Research in Computer-Aided Instruction indicates that student learning is greatly enhanced through the immediate presentation of relevant textual, static pictorial and graphic material. The learner's attention is not diverted from the learning task at hand if a control device is used to activate peripheral devices rather than the student performing such tasks himself. In addition, pictorial and graphic material can be inexpensively stored and easily retrieved via 35 mm slide or microfiche rather than if stored in computer memory.

Until multi-media student terminals, such as Bitzer's plasma-panel terminal, become widely available, there is an interim need to bring separate audio-visual devices under computer control, using the standard Modem (Modulator-Demodulator), the single voice-grade line, and an ASCII decoder as a control interface. It would be more convenient if the controller was a separate black box used to control different devices at different times, rather than part of the audio-visual device itself. This is especially apparent in small laboratories doing research on Computer-Aided Instruction, where it may be necessary to work with different combinations of these devices at different times.

At the time BTL undertook the design and construction of this kind of interface, it was commercially unavailable as a built-in or as a stand-alone unit. This report contains a description of the interface that was built and that is currently used in our laboratory.

The term ASCII is the common foreshortening of the United States of America Standard Code for Information Interchange. The ASCII code is commonly used with teletype installations for time-sharing computer systems. ASCII represents any one of 128 symbols, alphabetic characters, and numerals by a group of eight Binary digits (Bits). A group of binary digits is termed a Word. Teletype terminals in use at BTL are of the non-parity type. A parity system utilizes the eighth bit of the ASCII word to detect possible errors in data transmission. Non-parity systems always transmit the eighth bit of the ASCII words as a binary 1.

This report is to aid anyone wishing to construct a similar device for a similar application environment. With some minor modifications, this interface also could control several audio-visual devices simultaneously, or its logic could be extended to index more than a 100 item list.

SECTION II. SUMMARY DESCRIPTION OF THE ASCII DECODER

The computer-aided training of students frequently requires the use of supplemental graphics in the form of slides. An efficient selection and projection of such slides is via an ASCII decoder. The decoder receives alphanumeric characters from a remote time-sharing computer. The decoder then converts the ASCII bit pattern representing these characters to enabling and indexing pulses which activate the peripheral device. For example, the Eastman RAC 950 slide projector uses number-base nine digits to index any one of 80 slides. To place this device under the control of a program in a remote time-sharing computer, it is necessary to convert serial ASCII bit patterns to parallel signals representing base 9 integers. (In this case, since only 80 items are to be accessed, the interface can convert ASCII to a decimal base, and conversion to base 9 can be done by the programmer.)

Selection signals input to the decoder consist of three alphanumeric characters transmitted in an uninterrupted string. For example, the character string X^c67 is a selection signal for slide number 61 in the RA 950 projector. (A superscripted character, such as X^c, is a teletype symbol for the letter X transmitted with the Control Function Key depressed. The Control Function Key changes the seventh bit of the data stream from a binary 1 to a binary zero.)

The block diagram (Figure 1) shows that the pulse stream is tapped at the "receive" connection of the Modem, and is continuously monitored by the Control Gate decoder. X^c, selected since it is rarely used otherwise,

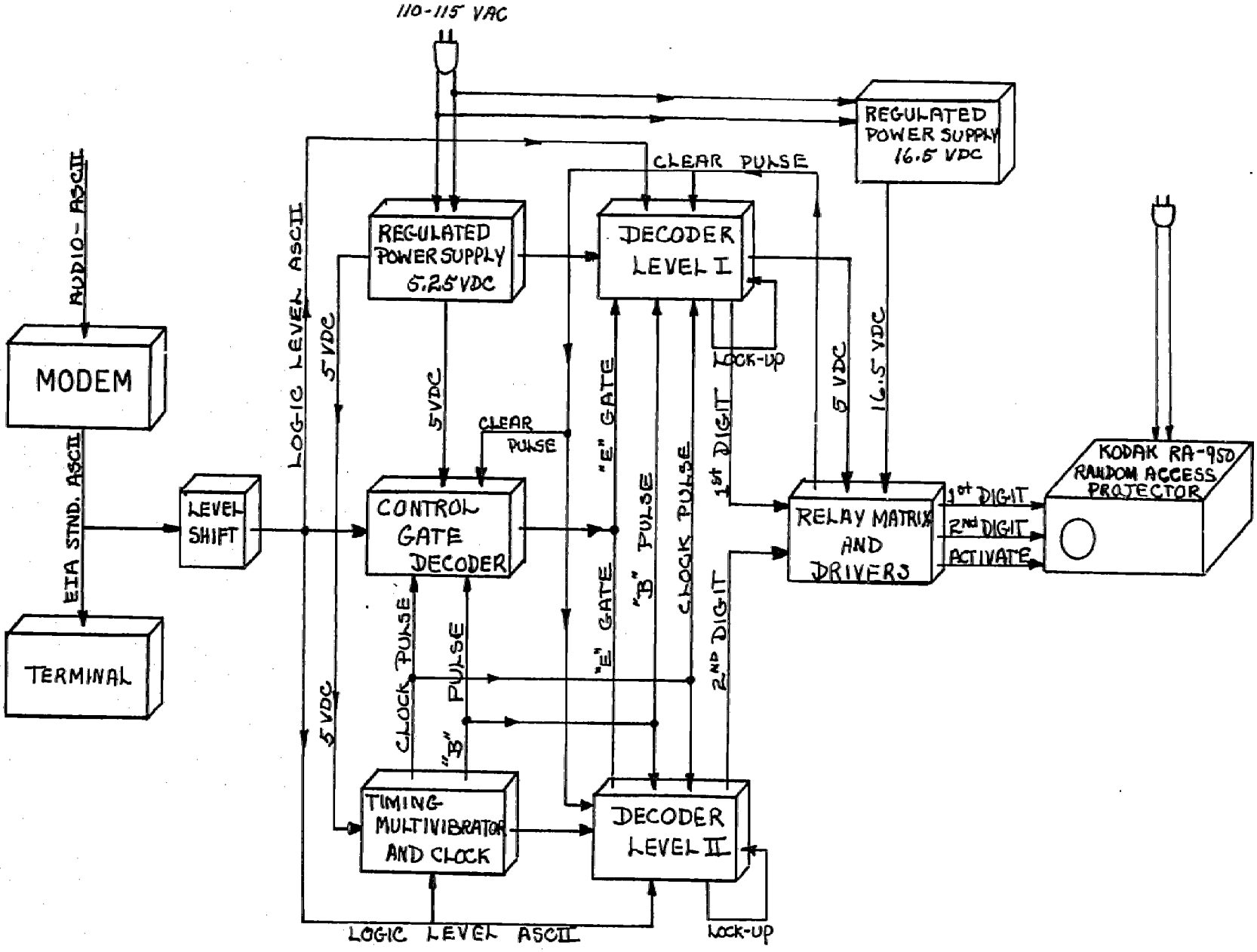


Fig. 1. ASCII Decoder Signal Flow Block Diagram.

is used to signal that the following pulse stream is to be decoded. Upon sensing X^c, the first numeric character of the string is gated to the Level I decoder. The serial pulses for this digit (0 to 9) are converted to parallel and held in a register until the pulse sequence for the second numeric character of the string is gated to the Level II decoder. This second pulse stream also is ASCII code for a digit from 0 to 9. It too is converted to parallel and registered. The sequences following these two pulse streams are blocked from entering the interface.

The bit pattern for each of the two digits is output in parallel from its respective register, and is converted to two signals representing digits from 0 to 9 and from 00 to 99. These two signals are amplified to activate the two relays in a 10 x 10 relay matrix corresponding to a number between 00 to 99. This number signifies which slide is to be pulled and projected by the Eastman RAC 950.

In this case, the indexing signals to the slide projector must be preceded by a signal to turn the projector on. After use, the projector may be turned off under program control. These actions are accomplished by selection of the matrix numbers 99 for ON, and 98 for OFF.

SECTION III. DESIGN CONSIDERATIONS

The ASCII decoder was designed as a separate "black box" that would perform as a basic unit for different applications with the minimum of additional circuitry.

Time-sharing computer systems utilize common (voice-grade) telephone lines for the transmission of data between computer and the remote terminal. At the time-sharing computer or the terminal, digital voltages or currents are converted to an audio frequency and modulated for transmission. Received acoustic signals are demodulated and converted to digital voltages or currents by the same device (Modem). Data is transmitted in an eight-bit binary code; the American Standard Code for Information Interchange (ASCII).

In the teletype terminal, data is received in the form of voltage or current pulses representing this eight-bit binary code. The character information is preceded by a one-bit long voltage pulse termed a "start pulse" which allows the teletype mechanism to synchronize with the data-stream. The data-stream is followed by a two-bit long pulse (negative voltage) termed a "stop pulse." During the stop pulse period the teletype mechanism mechanically selects and prints the chosen character (see Figure 2).

The total elapsed time for a single character selection is eleven units of time, equivalent to the duration of eleven bit pulses. Each bit pulse is approximately nine milliseconds long. Thus the transmission and reception sequence is: one start pulse, eight "data" pulses, and two

stop pulses, with a total elapsed time of approximately 99 milliseconds. This results in a character printing rate of approximately 10 characters per second for the standard electro-mechanical teletype. Electronic terminals may utilize character printing rates of 30 characters per second or higher. In these cases, bit time is proportionately reduced.

According to EIA standards, in this kind of signal transmission, the signal is to be considered in the marking condition when circuit voltage is more negative than minus three volts with respect to signal ground. The signal is in the spacing condition when the voltage is more positive than plus three volts with respect to signal ground. During data transmission the marking condition corresponds to binary one (hole punched in paper tape) and the spacing condition denotes binary zero. The marking condition (binary one) is the normal condition when no data signals are present on a circuit. Voltage rise and fall (transition) times should not normally exceed three percent of the nominal duration of a signal element (equivalent to the time required by one-bit pulse). Maximum signal voltage will normally not exceed twenty-five volts above or below signal ground.

Since Modem signal voltages generally exceed and are the inverse of those in Integrated Circuit (IC) logic, voltage conversion was necessary. (Logic circuits selected for the ASCII decoder operate at a maximum voltage of 5.25 volts positive above signal ground.)

Voltages selected for the ASCII decoder logic are:

1. More than 3.5 volts (nominal) positive above signal ground denotes binary one.

2. Less than .8 volts positive (nominal) above signal ground denotes binary zero.

The decoder was constructed of Integrated Circuits mixed with discrete components on circuit boards. These plug into standard connectors.

Three power supplies, two for the hybrid circuits and one for the relays, are necessary. All circuit boards are fitted into an enclosure which provides easy access to boards and components. The enclosure is perforated to provide ventilation for cooling.

SECTION IV. DESCRIPTION OF CIRCUITS

Overview of Circuit Functions

The ASCII Decoder is constructed with the circuits on individual plug-in circuit boards. These circuits are shown in logic diagrams (see Appendix B). Circuit boards are listed below:

Board 1 : Voltage level shifter and synchronization multivibrators

Board 2 : Timing components for synchronization circuits

Board 2a: Multivibrators and timing components for "activation" and "clear" pulse

Board 3 : Control (Entry) Gate Decoder

Board 4 : First digit (Level I) Decoder

Board 5 : Second digit (Level II) Decoder

Board 6 : Relay matrix drivers

Board 7 : Relay panel. (Boards 6 and 7 form a single unit that may be separated for troubleshooting or repair.)

Voltage Level Shifter and Synchronization Multivibrators

The output of the Modem is input to the ASCII Decoder through a Voltage Level Shifter, which shifts voltages to IC logic levels as previously described.

The ASCII pulse stream is monitored by the synchronization circuitry, comprised of a series of multivibrators. When no data is being transmitted, signal voltage output from the level shifter is approximately 5 volts (maximum 5.25 volts positive) and the synchronization multivibrators are in the quiescent (stable) condition.

The initial "bit" is the start pulse (taken at the output of the Level Shifter), or a voltage transition from +5 volts to a maximum of +.8 volts above signal ground. This voltage denotes a transition from the marking to spacing condition. The negative going edge of the pulse causes monostable multivibrator "A" to shift to its unstable state and produce a positive output of +5 volts for eleven milliseconds. At the end of the eleven millisecond period the multivibrator "A" shifts back to its stable state. The negative going edge of pulse "A" causes monostable multivibrator "B" to shift and produce a 5 volt positive signal for approximately 68 milliseconds (Figure 2).

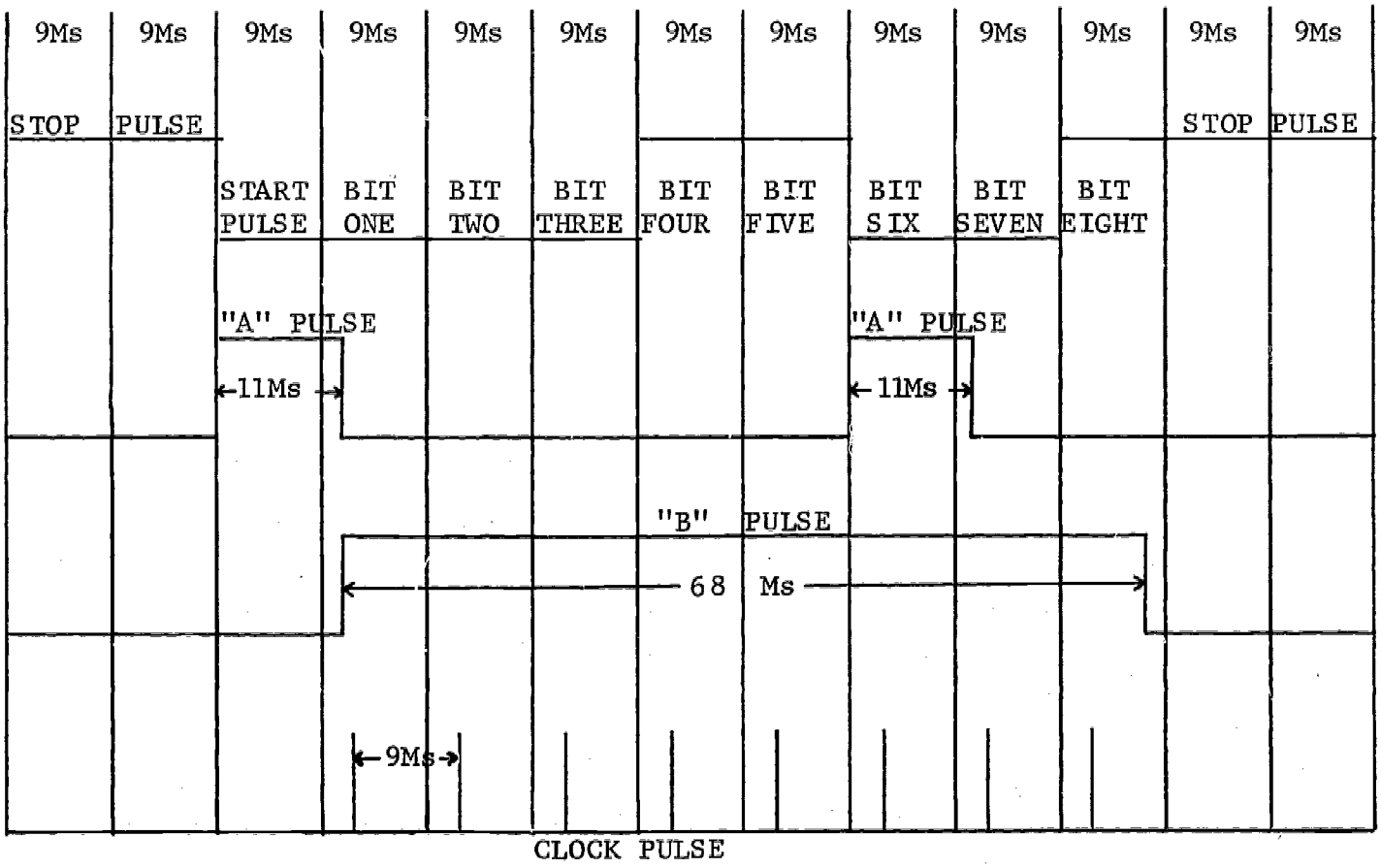


Fig. 2. ASCII Output and Synchronization Pulse Output. (LEVEL SHIFTER)

The positive going edge of the "B" pulse activates the "C" and "D" multivibrators to produce a 122 Hertz "clock" pulse. The "B" and clock pulses are routed to the Control Gate and Level I and II decoders to synchronize and gate the operations of these circuits.

Timing Components for Synchronization Multivibrators

The Monostable Multivibrators (MMV; Board 1) are timed by discrete components consisting of a fixed capacitor and variable resistor network (Figure 3). The variable resistor allows on-line adjustment of the MMV pulse width. In the prototype timing control is limited, however, timing can be extended to allow signal reception at a rate of 30 characters per second or higher to match the character reception rate of electronic terminals.

Multivibrators and Timing Components for Activation and Clear Pulses

After the ASCII data stream is decoded and the number matrix relays are activated, an activation multivibrator is enabled. This MMV produces a positive 5 volts pulse of approximately six seconds duration, which activates a relay within the RA 950 projector starting the slide tray drive motor. The negative-going edge of the activation pulse enables the "clear" multivibrator which produces a 50 millisecond 5 volt pulse which is fed back to the Control Gate and Level I and II decoders. This signal resets (or "clears") the decoder registers to the binary zero state. The registers are then ready to accept another selection signal.

The activation and clear MMV's are timed in the same way as the sychronization MMV's.

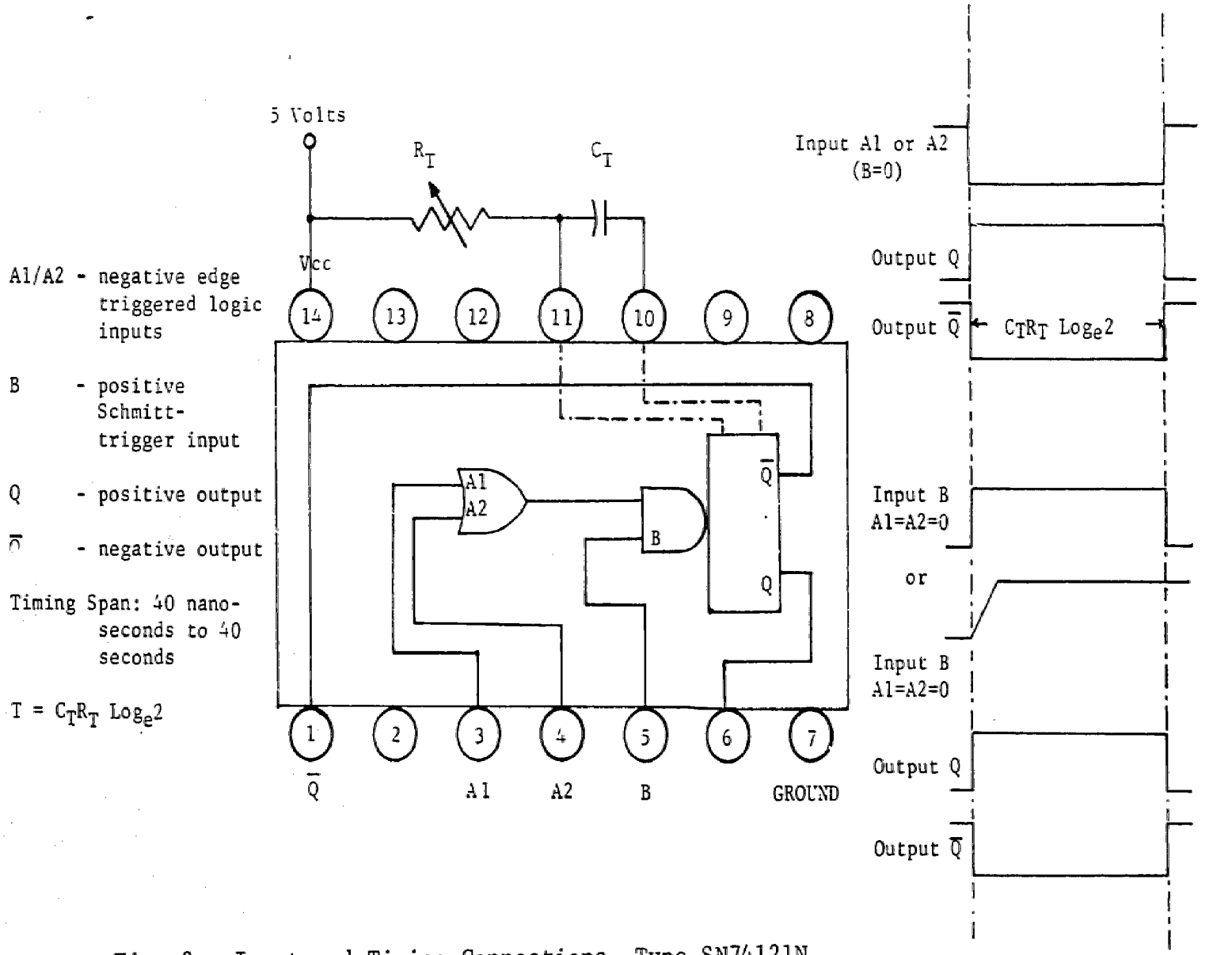


Fig. 3. Input and Timing Connections--Type SN74121N Monostable Multivibrator (Texas Instruments, Inc.) (Positive Logic)

Waveforms for SN74121N as a Monostable Multivibrator

Control Gate Decoder

This section enables a signal flow path to the digit (Level I and II) Decoders. It performs this function by sensing and decoding an otherwise unused ASCII character (X^c). When the signal path is enabled to the two digit decoders, the system is prepared to convert digits in ASCII code to decimal.

The Control Gate Decoder consists of self-complementing shift registers composed of Integrated Circuit R-S Master-Slave flip-flops, utilizing Transistor-Transistor Logic (TTL); and the TTL logic network of gates and inverters which sense the parallel output of the shift registers.

The "B" pulse from the synchronization MMV is routed to the control gate decoder, allowing the eight data pulses following the start pulse to enter the decoder circuits through AND gates. The "B" pulse is inverted to hold the decoder output at zero until the end of the 68 msec interval at which time all 8 bits of data have entered the shift register. This prevents transmitting transient states of the register to the digit decoders. This action results in the conversion of serially received data to a pattern stored in the register for parallel output.

The decoding of the entry character X^c gates the ASCII output of the Level Shifter to the Level I Decoder and simultaneously blocks further input to the Control Gate Register. The Register output remains stable until reset by the "clear" signal. This stable output is termed the "E" gate signal.

First Digit (Level I) Decoder

The first digit, or Level I, decoder senses a data stream only after the Control Gate Decoder produces an "E" gate signal as a result of the sensing and decoding of X^c.

The pulse form diagram (Figure 4) depicts the ASCII pulses received at the Control Gate and Level I Decoder. The "E" pulse opens the signal path for both ASCII and clock signals to the shift register. The serial input is decoded in parallel. The particular combination of binary zero's and one's is routed to a Binary Coded Decimal-to-Decimal converter which activates 1 of 10 outputs. Each output pin discretely represents one of the ten digits, 0 through 9. The selected decimal signal is then routed to a relay driving circuit located on circuit board 6. The last four bits of the data stream when decoded initiate a "lock-up" (D1) signal which prevents further input of ASCII or clock pulses.

Second Digit (Level II) Decoder

The signal path to the Level II decoder is enabled by the combined signals from the Control Gate Decoder ("E" Gate) and the Level I Decoder. Both must be present to gate ASCII and clock pulses to the Level II register. The necessary pulse forms are shown in Figure 5.

The Level II Decoder performs two actions. It first converts the binary coded signal to decimal in the same manner as Level I, and routes the decimal output to the second level of the relay matrix. A "lock-up" (D2) signal is also routed to the Activation Circuit (Board 2a) where it initiates the Activation signal after a built-in time delay of 50 milli-seconds.

Relay Matrix Drivers

The Relay Matrix Drivers are transistor circuits which allow current to flow through the solenoid coils of individual relays in the relay matrix. The output signals of Level I and II Decoders are reduced in voltage and applied to the transistor base causing the transistor to conduct current

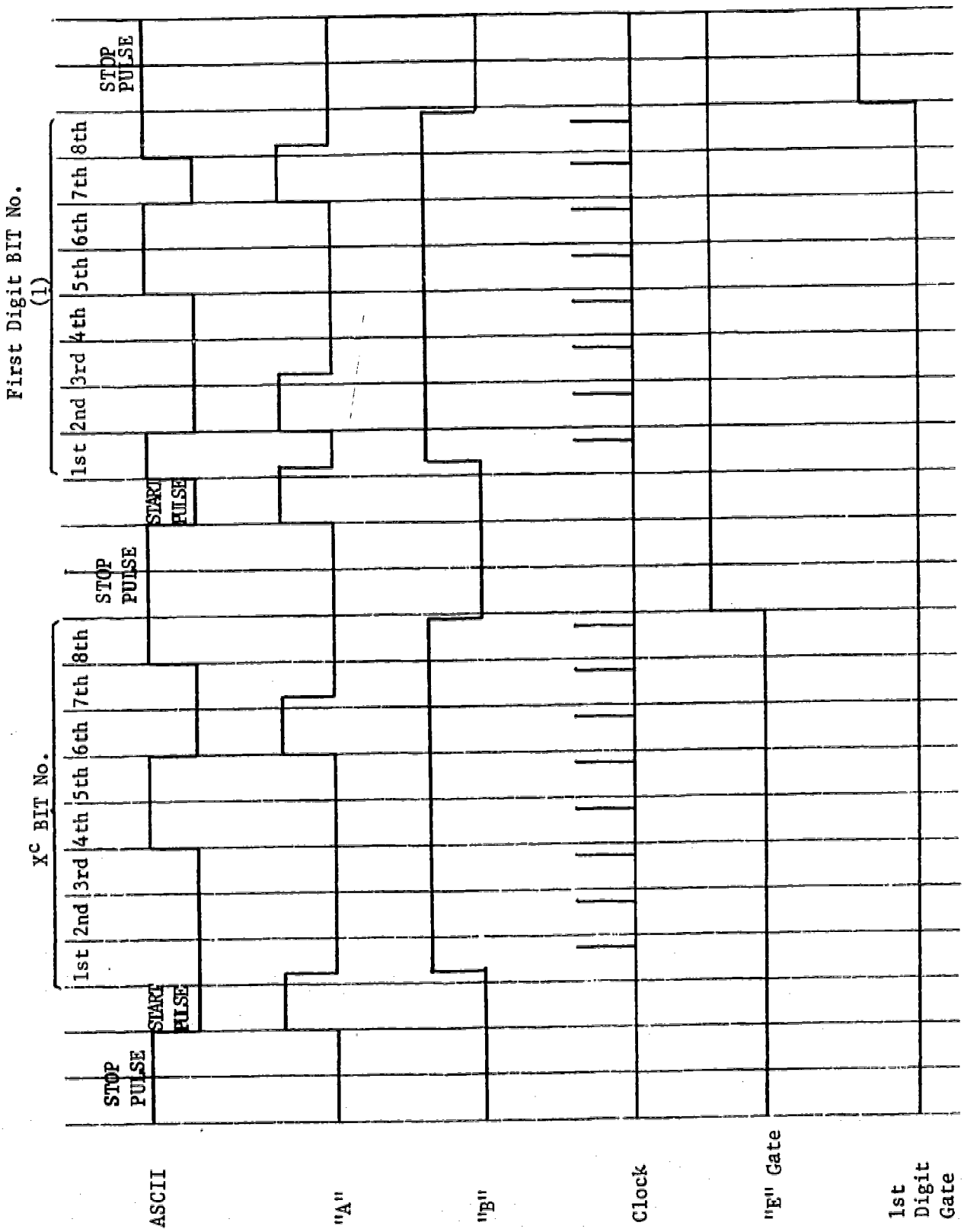


Fig. 4. Timing Chart--Control X and 1st Digit.

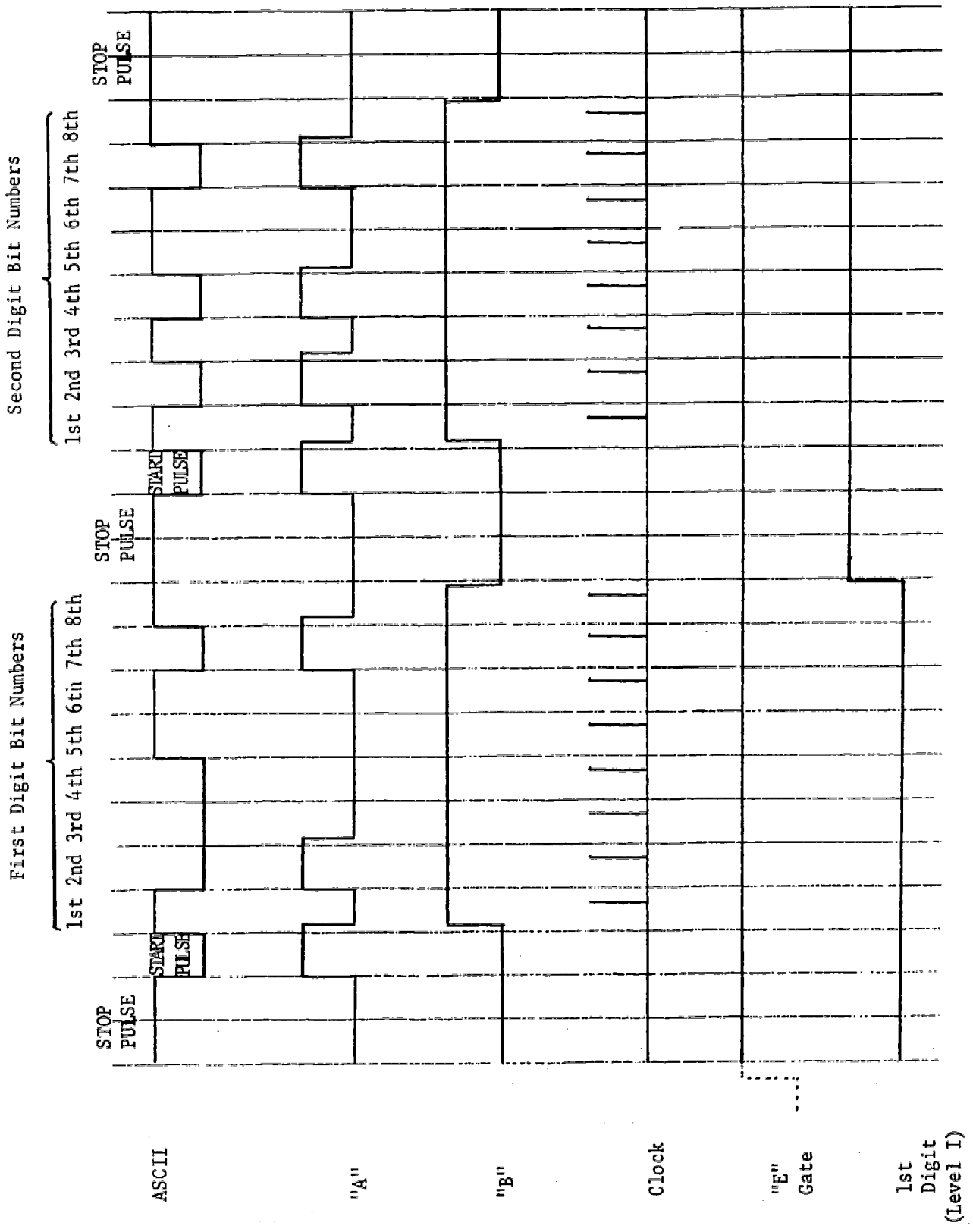


Fig. 5. Timing Chart--1st and 2nd Digit.

produced by an applied voltage of 16.5 VDC. The driver circuit action is analogous to closing a normally open switch.

The relay driver conducts current until the activation pulse terminates, at which time the "clear" signal resets the registers to the all zero condition which removes the signal from the transistor base. With the base signal absent, the driver blocks current flow to the relay coil.

Relay Panel

The Relay Panel contains twenty miniature multiple relays. When a relay driver is activated by a decimal output signal, the contacts of the relay close, creating a signal path to the RA 950 projector. Relay contacts remain closed for 6 seconds, a sufficient time for the projector drive system to position and project a slide. Relay contacts open when the "clear" signal resets the registers to the all zero state. Relays are designated by the digits zero through nine, and assembled into high-order and low-order groups. The desired high-order relay is the first activated by the Level I BCD/Decimal decoder. The activation of the desired low-order relay follows. The relay combination for selection of a desired slide may be found through the Selection Matrix Numeric Call Table in Appendix C.

The On/Off Control Circuit is shown in the Projector On/Off Circuit Schematic (Appendix A). The Latch relay is a two element, momentary solenoid which mechanically locks into either the open or closed position. Once signalled closed the contacts remain closed until positively signalled open.

Detailed Technical Description of Circuit Functions

Voltage Level Shifter

The Voltage Level Shifter utilizes a Texas Instruments Quad Line Receiver Type SN75154N. This integrated circuit is specifically designed to accept EIA standard voltages and convert them to logic levels. Only one of the four individual level-shift circuits combined in the package is necessary to the circuit. Should a malfunction occur in a sub-circuit, repair is easily accomplished without replacement by simply shifting connections to an unused level-shift circuit in the installed package.

Operation of the level-shift circuit is from a positive 5 volt D.C. power supply. Its internal logic is Bipolar Transistor-Transistor. The level-shifter is capable of driving ten type 54/74 integrated logic devices without degrading its operation.

Synchronization (Timing) Circuits

Timing and synchronization is performed by type SN74121N integrated circuit, Monostable Multivibrator (MMV) operated from a 5 VDC power supply. Each MMV is individually timed with a variable resistance network and a fixed polarized capacitor. The variable resistance allows adjustment of the output pulse width necessary for initial synchronization alignment.

In the prototype, timing control is limited to the narrow band necessary for alignment. Should the decoder be desired for a wider range of usage and the interpretation of signals transmitted at varying baud rates, timing control may be easily extended.

Timing is determined by the following function in the SN74121N.

$$T = C_t \times R_t \, \mathrm{Log}_e 2$$

C_t is in microfarads, R_t in kilohms and T is in seconds. Timing components are applied as shown in Figure 2.

The Clock Pulse Generator consists of two SN 74121N MMV's connected in a stable gated configuration. Each MMV is individually timed as previously described. The resulting waveform may therefore be controlled in individual pulse widths and pulse rate. Figure 6 depicts the interconnections necessary to provide the stable "clock pulse" waveform.

Synchronization and timing are major considerations in the conversion of binary coded ASCII data to discrete function signals. All switching circuits, registers, and gates must sense only the eight bits lying between the start and stop portions of the signal stream. To accomplish this, circuits must be made insensitive to those portions of the signal which do not carry the basic intelligence.

The time related characteristics of the ASCII code were originally determined by the electrical and mechanical character of the teletype terminal. Bit duration was constrained by the mechanical lag of the teletype's internal parts. To utilize the ASCII signal electronically, the decoding circuits must not respond to the start pulse or stop pulse. Since a start pulse always follows a stop pulse, the negative transition of the signal at the beginning of the start pulse provides a convenient point of reference for timing. The "A" MMV responds to all negative going logic level voltage changes. Its "ON" period is set at eleven milliseconds, or slightly longer than the duration of the start pulse. The negative going edge of the "A" pulse initiates the "B" pulse, which always goes positive 2 milliseconds after the occurrence of the first bit time period. The "B" pulse starts the clock, and also enables the signal path to the Control Gate Decoder. The "B" pulse is positive for about 70 milliseconds, and terminates just prior to the end of the eighth-bit time period. The "A" MMV may respond to a negative going edge of the ASCII pulse several

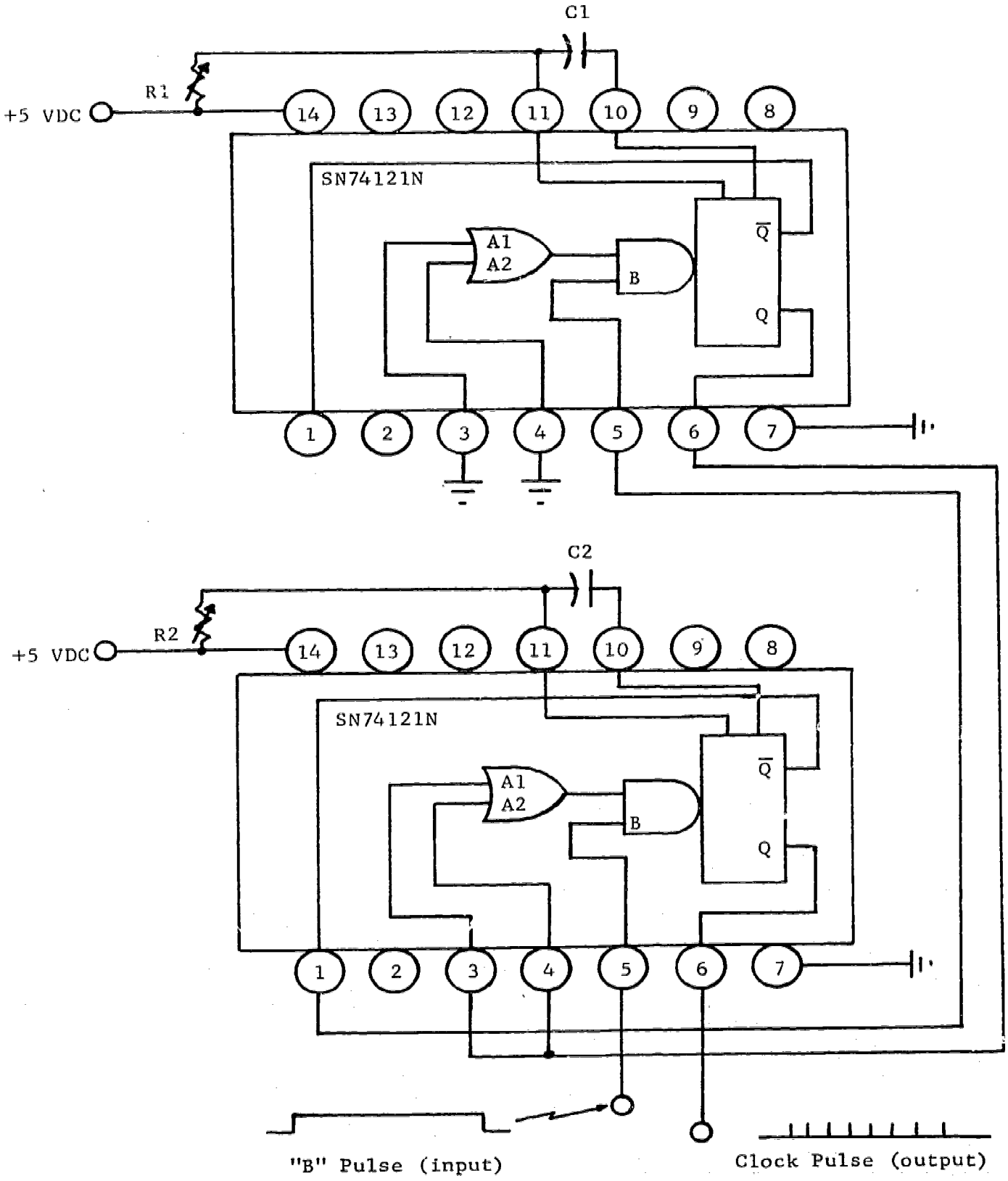


Fig. 6. Clock Pulse Generator 2/SN74121N in Stable Gated Configuration.

times during the period that the "B" pulse is positive, dependent upon the varying states of the ASCII code. This does not affect the activity of "B" MMV, which is responsive to the "A" pulse only when in its stable state (see Figure 4). The "B" pulse, then, differentiates the intelligence carrying portions of the ASCII from the timing portions, and routes this portion to the desired circuits.

Control Gate Decoder

The Control Gate Decoder utilizes two SN7496N R-S, 5-bit shift registers (sometimes termed a 5-bit latch) connected in series to act as a 10-bit register, and to convert serially input data to parallel output for decoding (Figure 7). Operating from 5 VDC, these integrated circuits were selected because they can be reset to an all-zero binary state with the application of a single input signal. A 5-bit shift register consists of five cascaded flip-flops (F/F). The binary state present as input to the first F/F is transferred to its output by the rising edge of a clock pulse. The output of the first F/F is the input to the second F/F, the second to the third, and so on. The serially received data stream is entered sequentially into the first shift register, and is shifted through the register until eight bits have been received. These eight bits, represented as outputs, (one bit at each of the eight flip-flops), are available for parallel decoding by appropriate logic. Truth Table 1 displays the binary states of each of the shift register flip-flops for each sequential unit of time. The state shown is that immediately following the rising edge of the clock pulse.

The Control Gate register retains the X^C binary pattern as its output, but ignores any other alphanumeric or control characters. When the binary

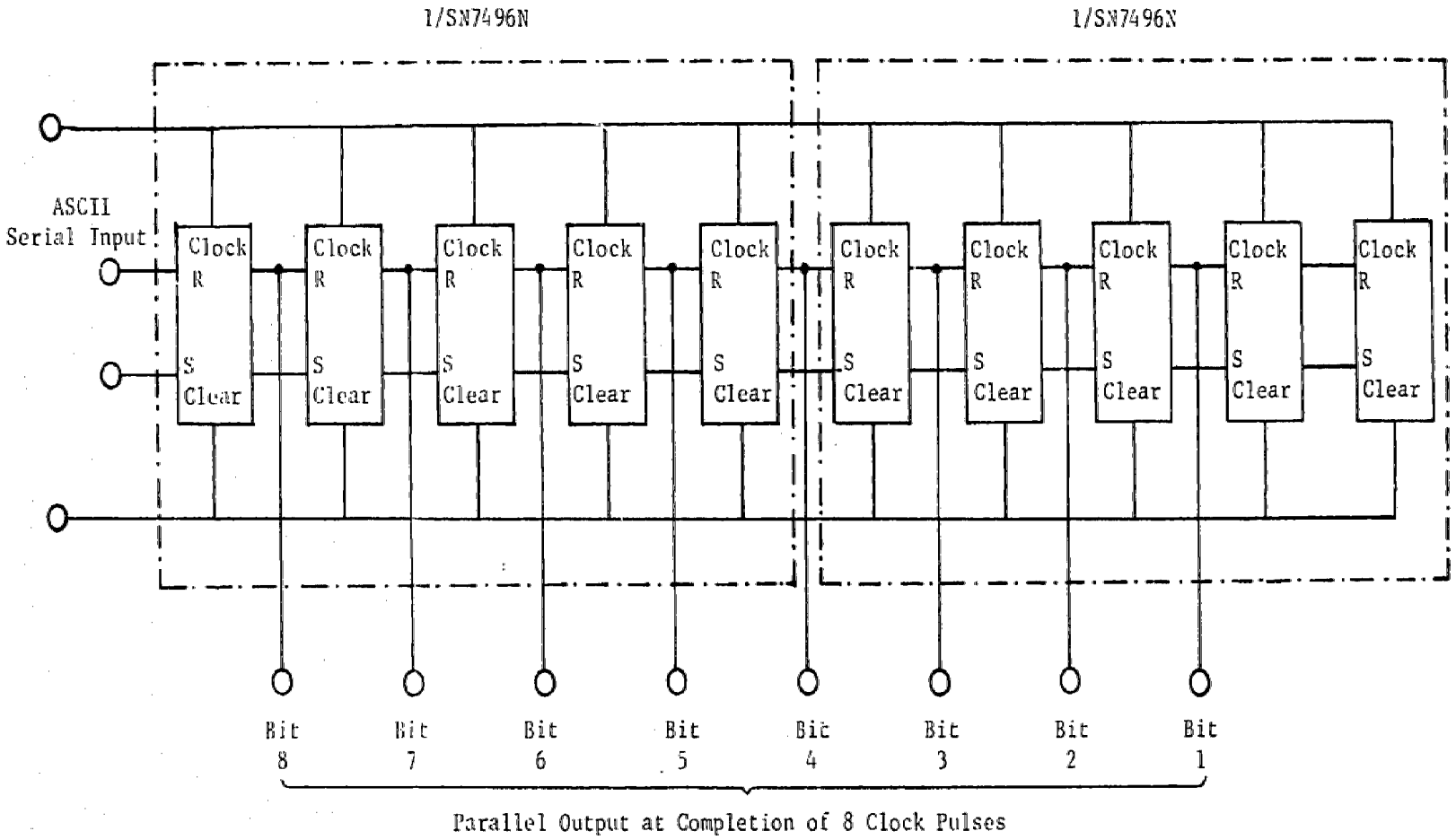


Fig. 7. Decoder Register--2 SN7496N in Series (see Table 1 for Truth Functions).

Table 1

Truth Table for Entry Gate Decoder Section for the Receipt of Character X^c (bit pattern 00011001)

		Binary Voltage Output of Flip/Flops No. 1	2	3	4	5	6	7	8	
Serially Received Bits	First	0	0	0	0	0	0	0	0	
	Second	0	0	0	0	0	0	0	0	
	Third	0	0	0	0	0	0	0	0	
	Fourth	1	0	0	0	0	0	0	0	
	Fifth	1	1	0	0	0	0	0	0	
	Sixth	0	1	1	0	0	0	0	0	
	Seventh	0	0	1	1	0	0	0	0	
	Eighth	1	0	0	1	1	0	0	0	
		8th	7th	6th	5th	4th	3rd	2nd	1st	Bit received*

pattern for X^c is received and retained, the signal path to the Level I digit decoder is enabled by the "E" Gate pulse.

All output from the Control Gate is suppressed during the occurrence of the "B" pulse to prevent providing false "E" gate signals to Level I or Level II decoders while the register is cycling.

Decoding of the ASCII binary character X^c is accomplished with logic circuitry that responds only to a specific bit pattern. The basic logic for decoding is shown in the Logic Diagram, Appendix B.

*Note that the bit pattern is stored in inverse order of receipt. The 1st bit received is stored in register No. 8, the last bit received in register No. 1.

The signal paths for ASCII and clock pulses to the Level I Decoder are enabled by the "E" gate output from the Control Gate Decoder. The Level I Decoder utilizes a register system precisely the same as that of the Control Gate. The decoding logic that follows the register responds to the ASCII bit patterns for the digits 0 through 9 rather than to a discrete pattern such as X^C.

The logic for digit (decimal) decoding is, by necessity, quite different from that used in the Control Gate Section. The actual conversion of the binary data is accomplished by an integrated circuit type SN 7442N, whose logic is depicted in Figure 8.

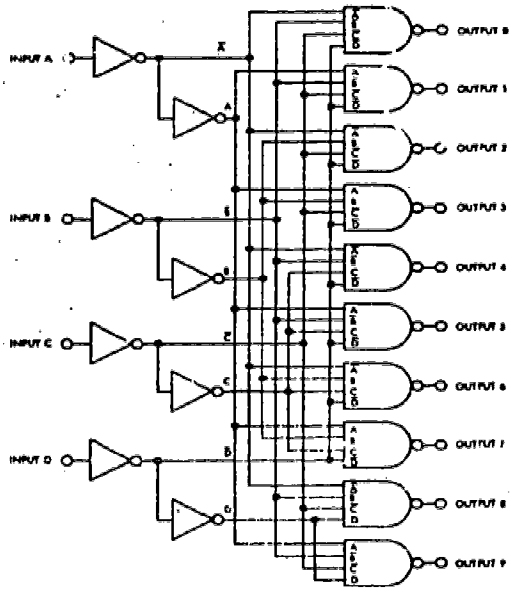


Fig. 8. SN5442/SN7442 BCD-to-Decimal.

This circuit decodes a 4-bit word to produce a logic ONE output on one of the ten output lines. The 4-bit word consists of the first four serially received bits of the ASCII data representing a particular digit.

The pattern of the last four bits of the ASCII code for a digit is always the same (bit pattern: 1101) regardless of the digit transmitted in a non-parity system.

The logic diagram for the Level I decoder is shown in Appendix B. Decoding is accomplished in the following sequence. With input gates enabled by the "E" pulse, the ASCII data sequence for a digit (0 through 9) is gated into the G1 register. This takes about 99 milliseconds. During this time, the outputs from all AND gates are maintained at a binary zero, and the BCD to Decimal decoder receives no inputs from the register.

A binary word of N digits in length can form 2^N different combinations. In the case of a 4-bit word input decoder, 2^4 (16) binary words may be decoded. The SN 7442 BCD-to-Decimal decoder decodes only 10 of the 16 possible binary digit combinations. Table 2 depicts the output of the circuit for the possible 4-bit word inputs.

When the Level I register is in a static condition, that is, not holding an ASCII digit, the input to the BCD-to-Decimal decoder is 0000. This condition is decodable and will produce a binary zero at output pin 0. This condition is unacceptable, for it would result in the activation of the decimal 0 relay during all static periods of the decoder unit.[1]

A special logic circuit (Figure 9) interposed between pin 0 of the BCD-to-decimal decoder and the decimal zero relay prevents this erroneous

---

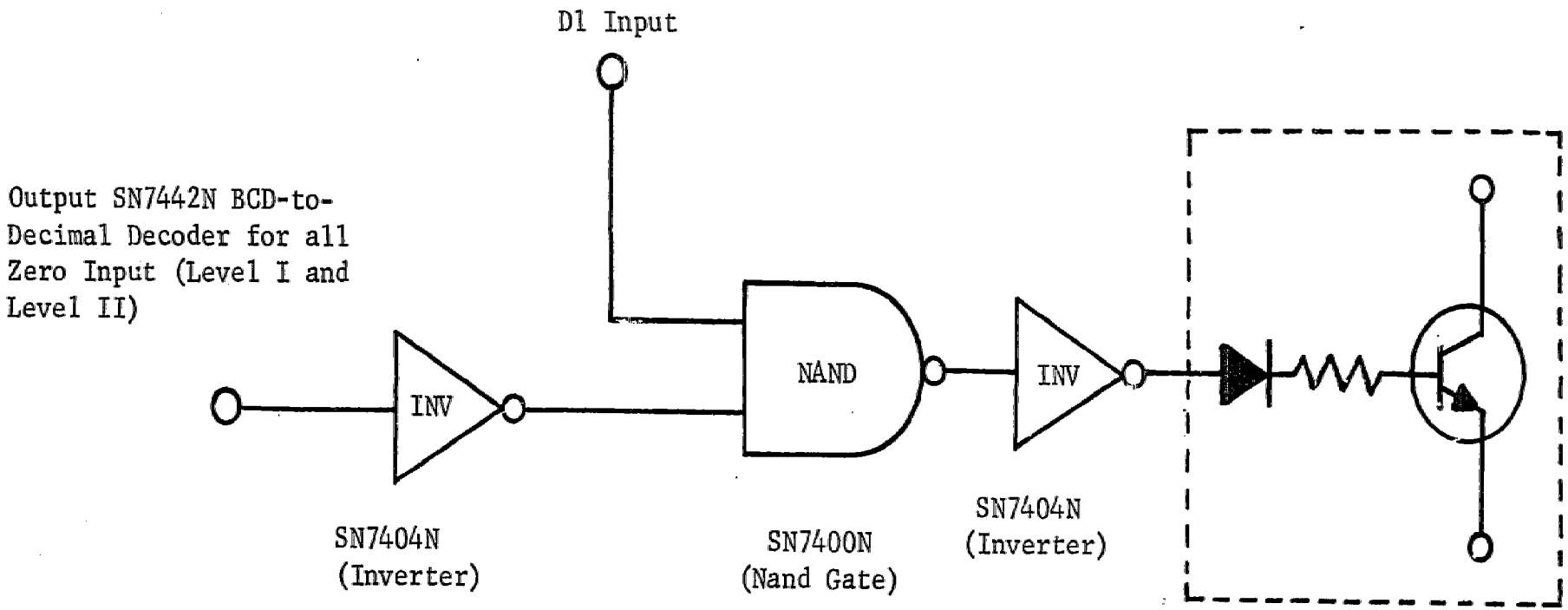
[1]The BCD/Decimal decoder utilizes negative logic, i.e., a positive voltage output is considered a Binary Zero, an output voltage of zero is considered a Binary One.

Table 2

Truth Table BCD-to-Decimal Decoder (SN 7442N)

	A	B	C	D	0	1	2	3	4	5	6	7	8	9
	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	1	0	0	0	1	0	1	1	1	1	1	1	1	1
	0	1	0	0	1	1	0	1	1	1	1	1	1	1
	1	1	0	0	1	1	1	0	1	1	1	1	1	1
	0	0	1	0	1	1	1	1	0	1	1	1	1	1
	1	0	1	0	1	1	1	1	1	0	1	1	1	1
	0	1	1	0	1	1	1	1	1	1	0	1	1	1
	1	1	1	0	1	1	1	1	1	1	1	0	1	1
	0	0	0	1	1	1	1	1	1	1	1	1	0	1
	1	0	0	1	1	1	1	1	1	1	1	1	1	0
Normally Unused as Inputs	0	1	0	1	1	1	1	1	1	1	1	1	1	1
	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: All outputs remain off for all invalid inputs; Negative Logic is utilized. Off condition is represented by Binary ONE.



TRUTH TABLE		
BCD/Decimal	D1 or D2	Input to Relay Driver
0	0	1
1	0	1
0	1	0

Fig. 9. Special Input Circuit to Level I and Level II First (Digit Ø) Relay Drivers to Prevent Relay Activation in the Static (Non-selected) State.

activation, but allows proper activation when the ASCII code for digit zero has been loaded into the shift register.

At the completion of the register loading cycle, the 8-bit word representing the digit is processed as two separate 4-bit words. The first 4-bit word is decoded by the BCD/Decimal decoder, the second 4-bit word is decoded by ANDing to produce a 1st digit (D1) signal. The D1 signal blocks further ASCII or clock inputs to the register, which will maintain its output state until reset to the all zero condition. The D1 signal, in conjunction with the "E" pulse, now enables the second digit (Level II) decoder. The BCD/Decimal decoder produces a selected output to activate the required relay of the Selection Matrix.

Second Digit (Level II) Decoder

The Level II decoder duplicates the function and circuitry of the Level I circuit. The output from the Level II BCD/Decimal decoder is dependent on the first 4 bits and is used to activate the selected relay at Level II of the Selection Matrix. The last four bits are used to generate the second digit (D2) output pulse which blocks further ASCII or clock inputs to the register. All inputs to the decoder circuits are now blocked until the projector completes its selection cycle.

Relay Matrix and Driver Circuits

Relays normally have activating voltage and current requirements that exceed the operating capabilities of TTL I.C. logic. Therefore, it is necessary to procude a separate power supply for relay operation, and individual circuitry to route power to a relay which has been selected for operation.

Each of the twenty relays of the selection matrix has an individual driver network that responds to TTL logic voltage signals. The driver circuit is shown schematically in Appendix A, page 34. Matrix relays, Elgin type MN7217, are shown schematically in Appendix A, page 35. Contacts for this type of relay will carry 1.0 amperes at 26.5 VDC. Drivers are supplied with 16 VDC (regulated) at an operating current of 50 milliamperes. This is the minimum voltage for positive relay action. Reduced voltage is utilized to increase external circuit life and reduce heating. Relays may remain activated for an indefinite period at these operating levels without damage.

Selection Activation

The onset of the Level II decoder digit signal D2 is an indication that the three decoders (Control Gate, Levels I, and II) have received and decoded a three character set of symbols for slide selection. The D2 signal triggers an MMV which produces a 50 millisecond delay pulse. This delay is provided to allow time for positive closure of the relay contacts before signalling activation. The negative-going edge of the delay pulse drives the activation multivibrator to a positive output. This 6-second duration activation pulse is routed to the Activation Relay Driver which closes the contacts of the activation relay. The activation relay circuit in turn signals the RA 950 projector to operate the tray drive and seek a new slide for projection. A new slide will be projected in less than 4 seconds. At the end of the six second activation pulse, the negative-going edge signals the register "clear" multivibrator to generate a negative-going pulse of 50 milliseconds duration. The clear pulse acts to reset all registers to the all-zero output condition. These waveforms

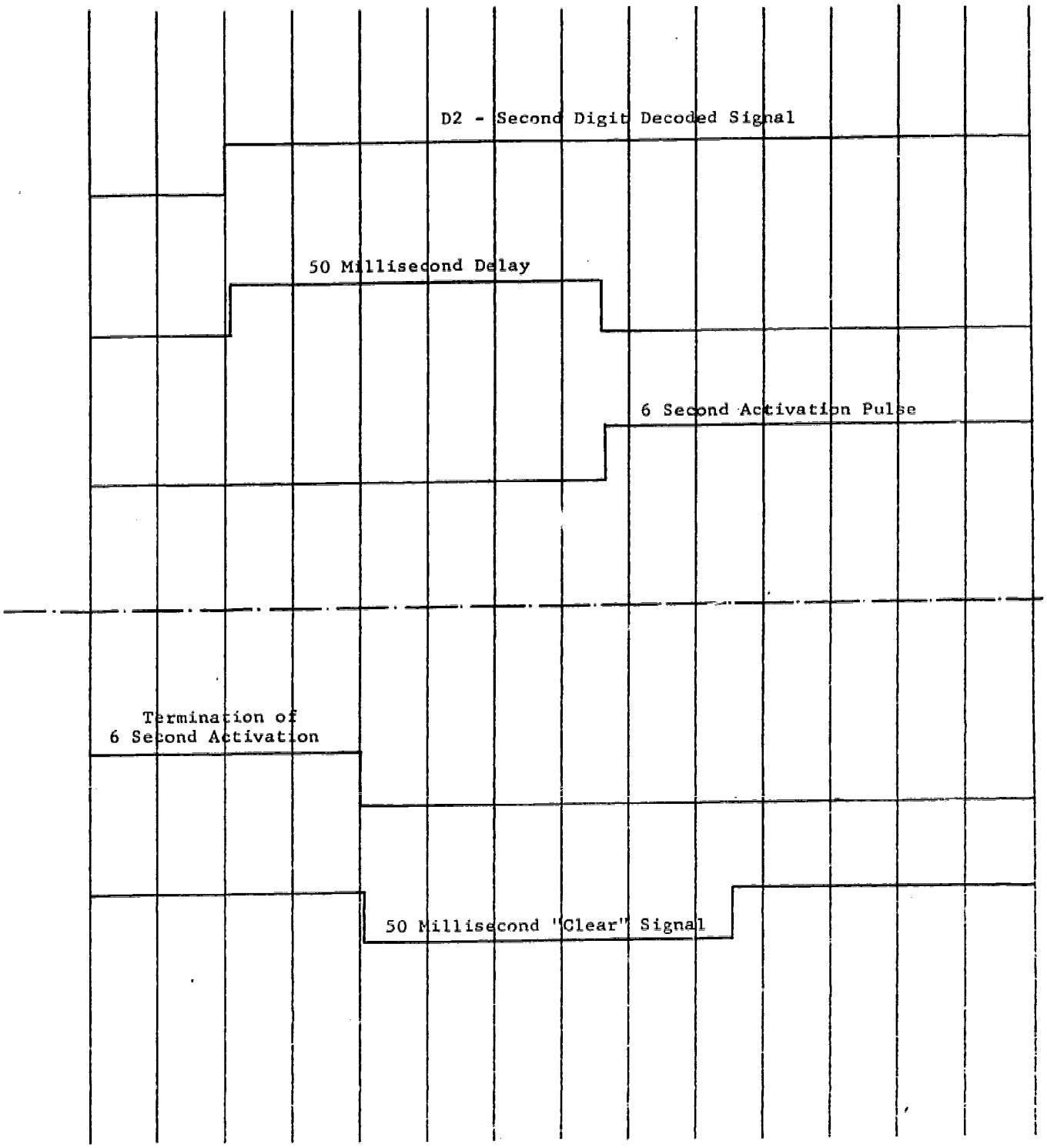


Fig. 10. Timing Chart for Activation and Clear Pulse.

are depicted in the timing diagram (Figure 10). In this condition, the Control Gate decoder is awaiting a new selection command from the Modem.

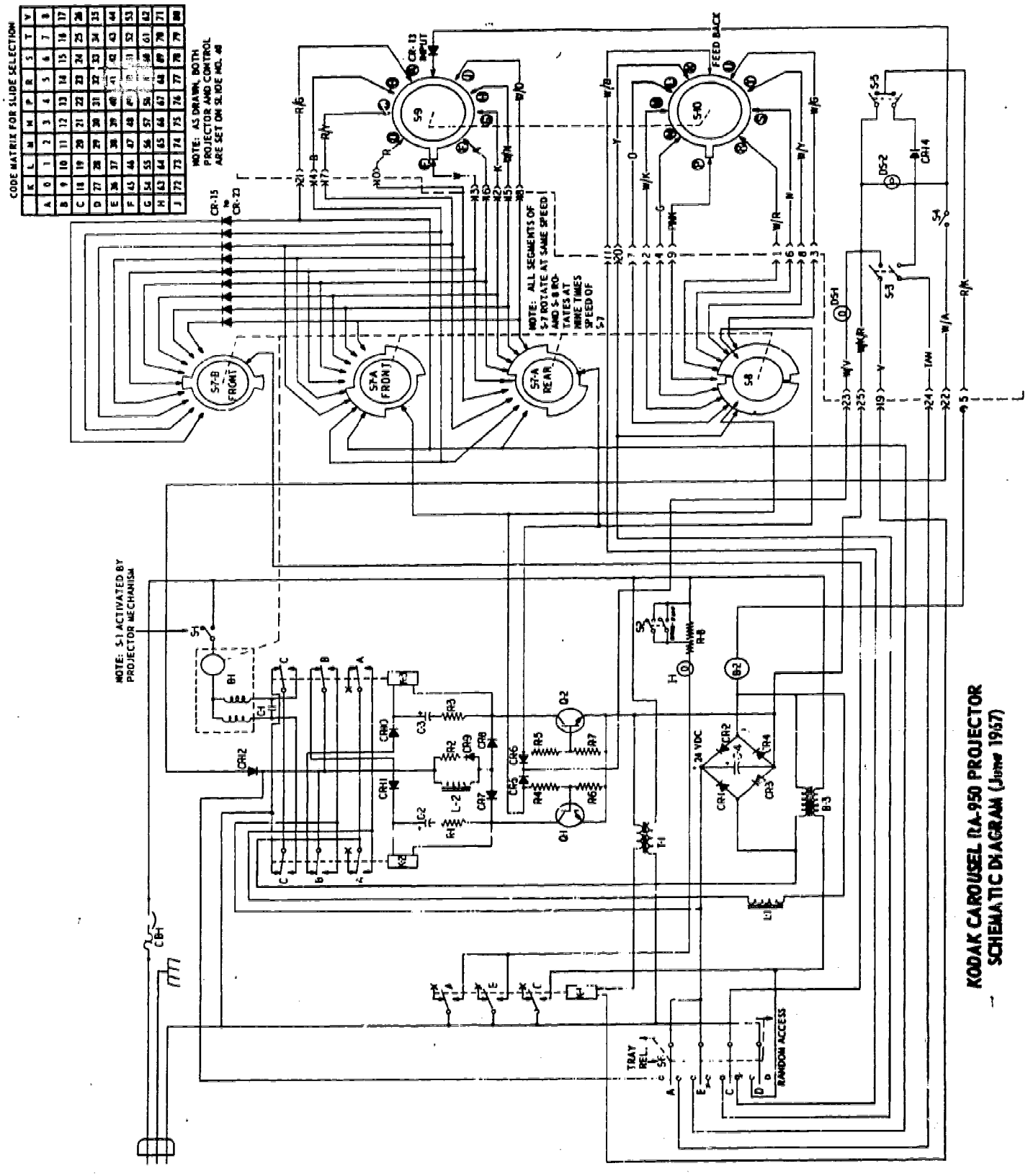
Projector ON/OFF Circuit

The ASCII decoder has the capability of placing the RA 950 projector into or out of operation. Only 81 of the possible 100 base ten numbers are needed to select and project slides, since the slide tray has only 81 slots. Decimal 99 has therefore been hard-wired to provide an ON signal that routes voltage to the projector circuits through a latching relay. Similarly, decimal 98 will, by resetting the latching relay, cause the projector to go out of operation.

The latching relay can be reset to OFF should program control be lost, by opening the enclosure and moving the mechanical latch to the open position. A momentary contact switch will be added to the present circuitry to allow manual control of the ON and OFF functions without opening the enclosure. (See General Schematic: APPENDIX A).

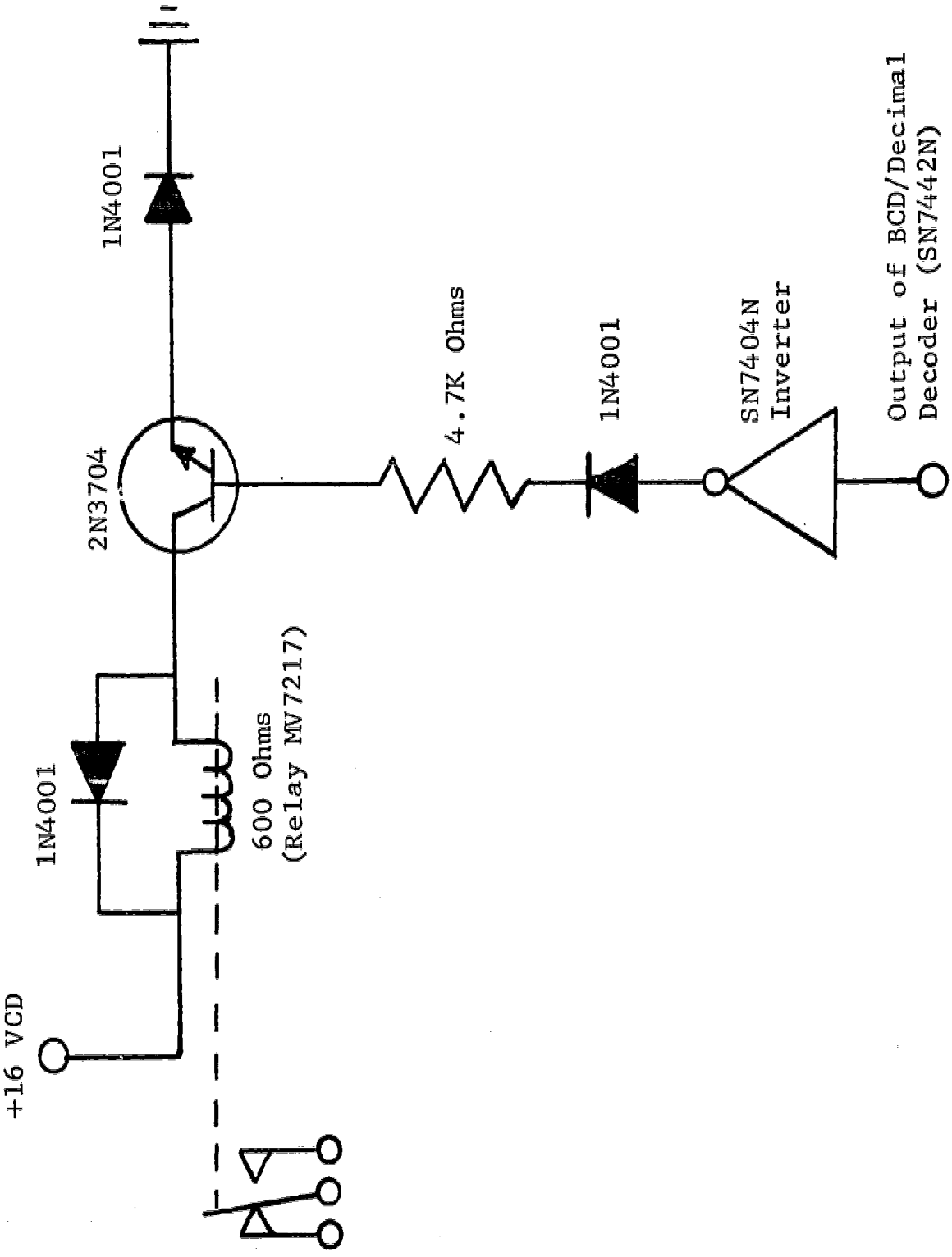
APPENDIX A

SCHEMATICS

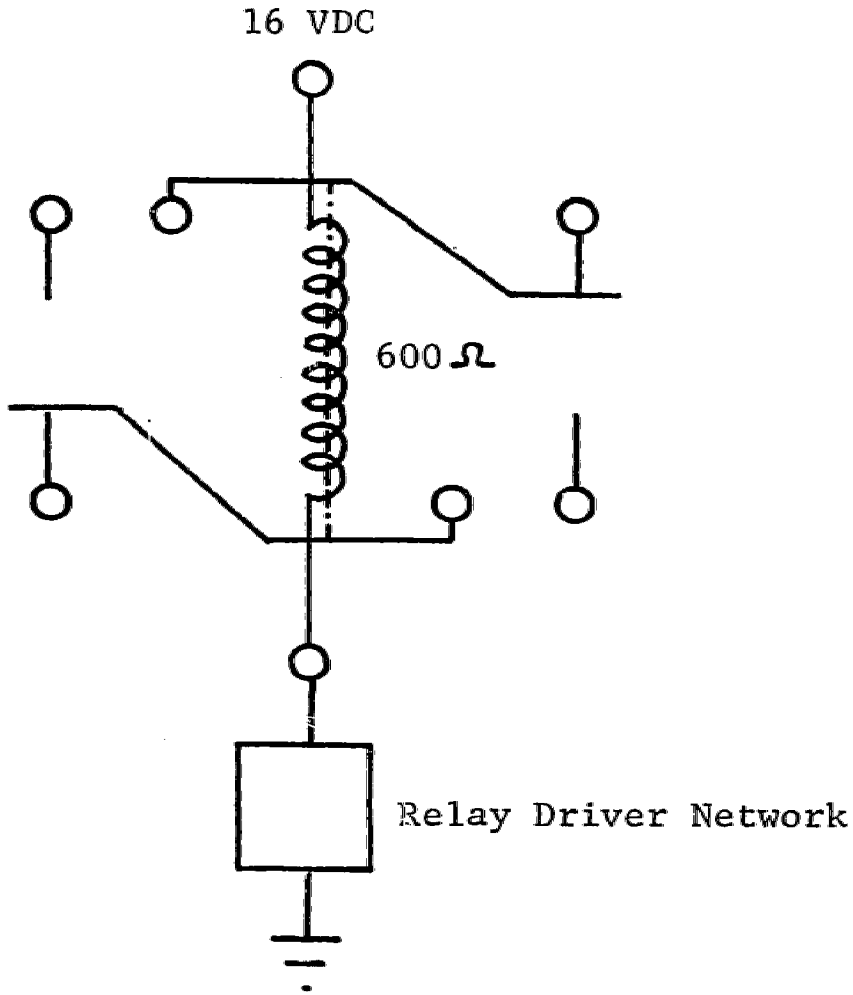


KODAK CAROUSEL RA-950 PROJECTOR
SCHEMATIC DIAGRAM (June 1967)

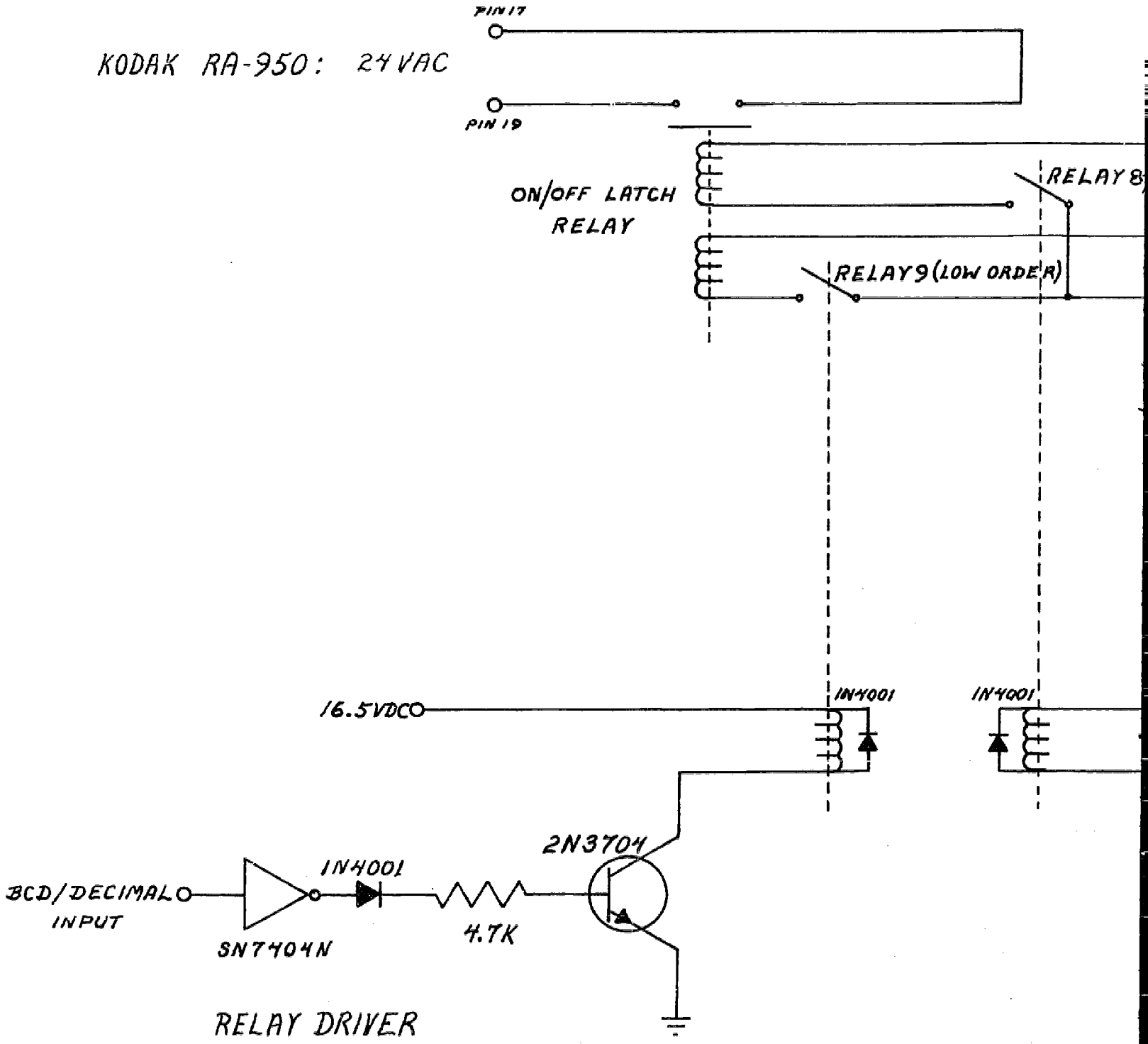
RELAY DRIVER SCHEMATIC



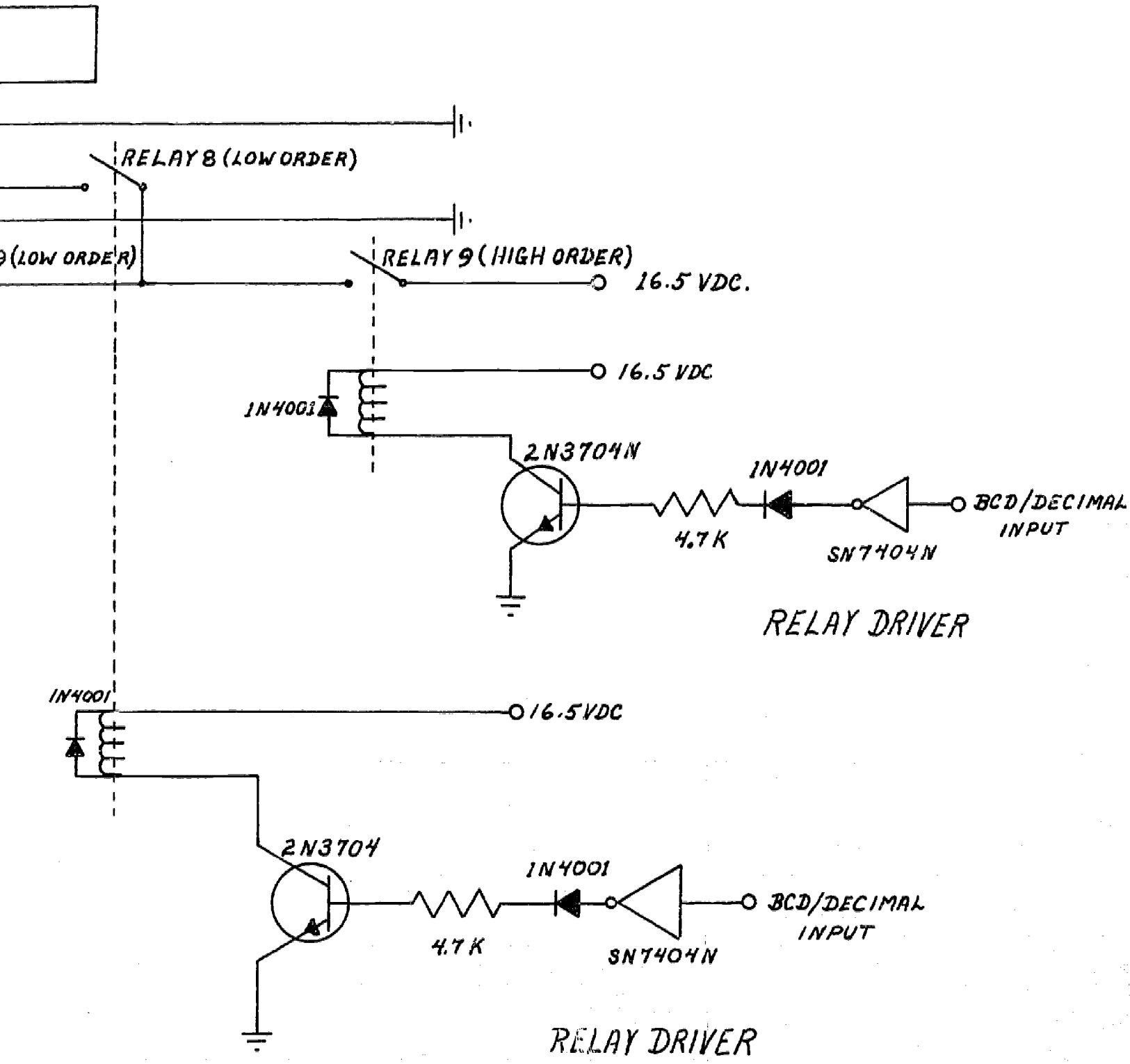
ELGIN RELAY MV7217 SCHEMATIC



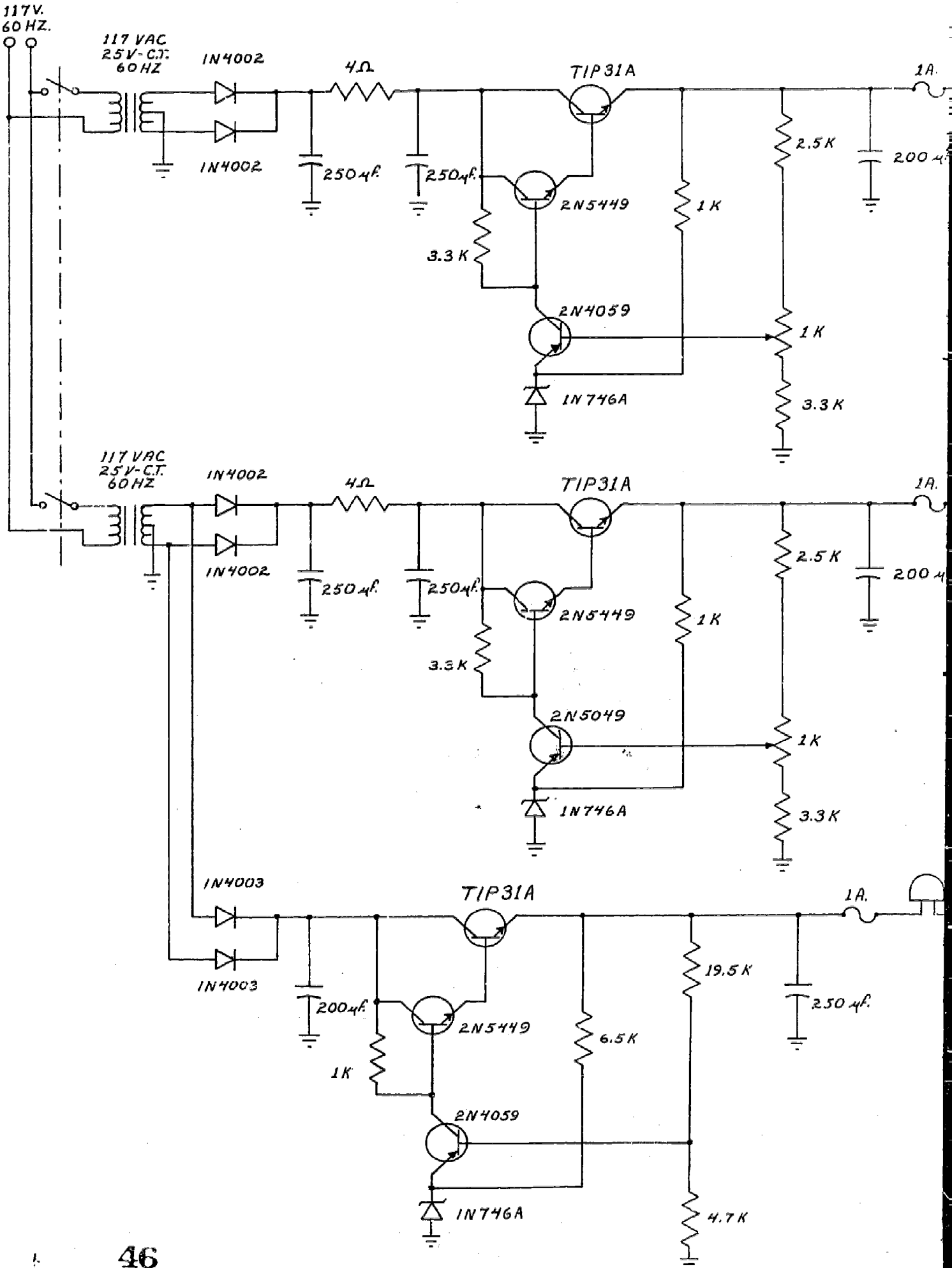
Note: Both contact elements close simultaneously when relay activated.

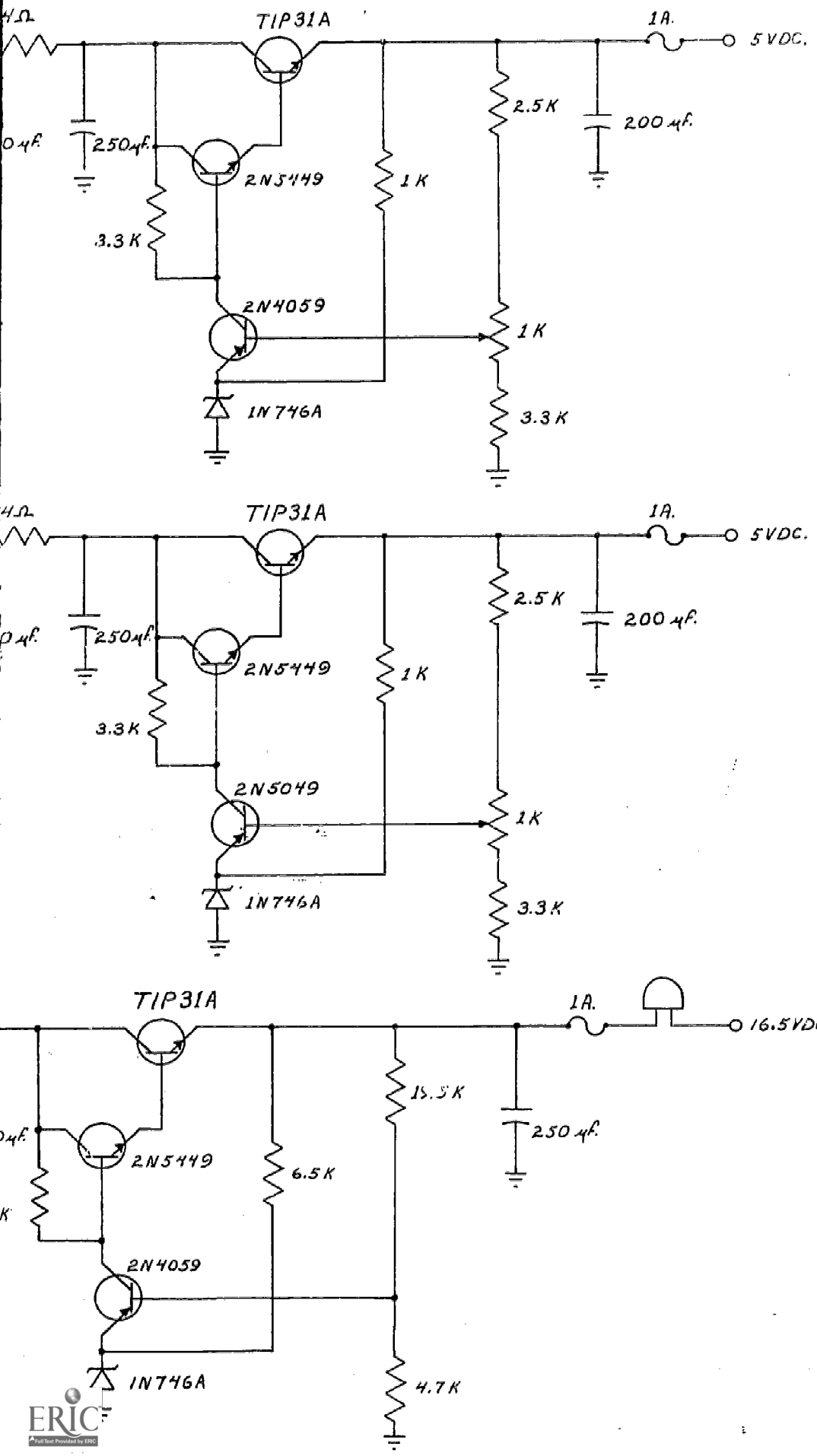


PROJECTOR ON/OFF CIRCUIT - SC



F CIRCUIT - SCHEMATIC


117V.
60 HZ.
117 VAC
25V-C.T.
60HZ
IN4002
IN4002
4Ω
250μf.
250μf.
TIP31A
2N5449
3.3K
2N4059
IN746A
1K
2.5K
1K
3.3K
200μf.
1A.
117 VAC
25V-C.T.
60HZ
IN4002
IN4002
4Ω
250μf.
250μf.
TIP31A
2N5449
3.3K
2N5049
IN746A
1K
2.5K
1K
3.3K
200μf.
1A.
IN4003
IN4003
200μf.
TIP31A
2N5449
1K
2N4059
IN746A
6.5K
19.5K
4.7K
250μf.
1A.

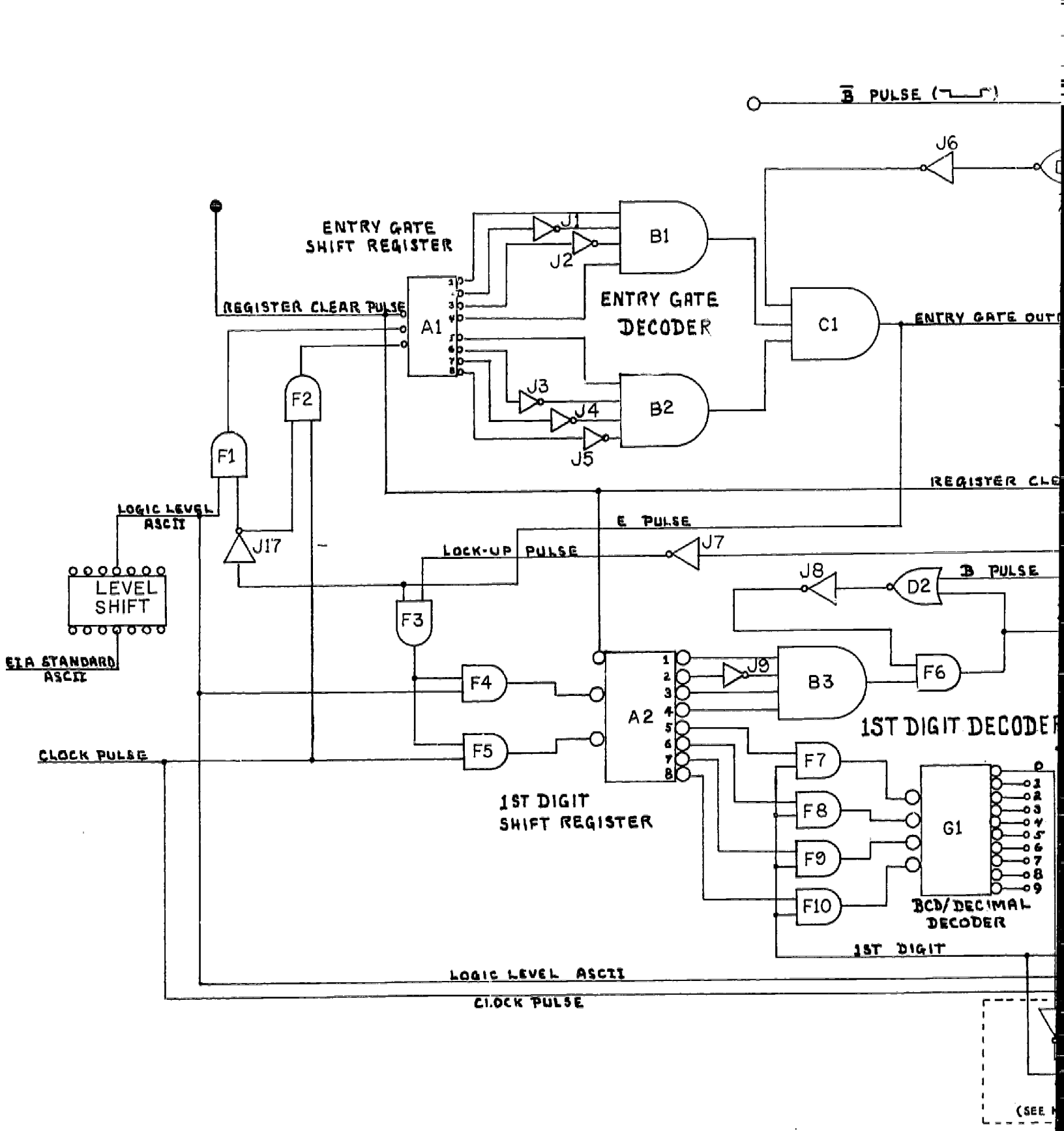


POWER SUPPLY

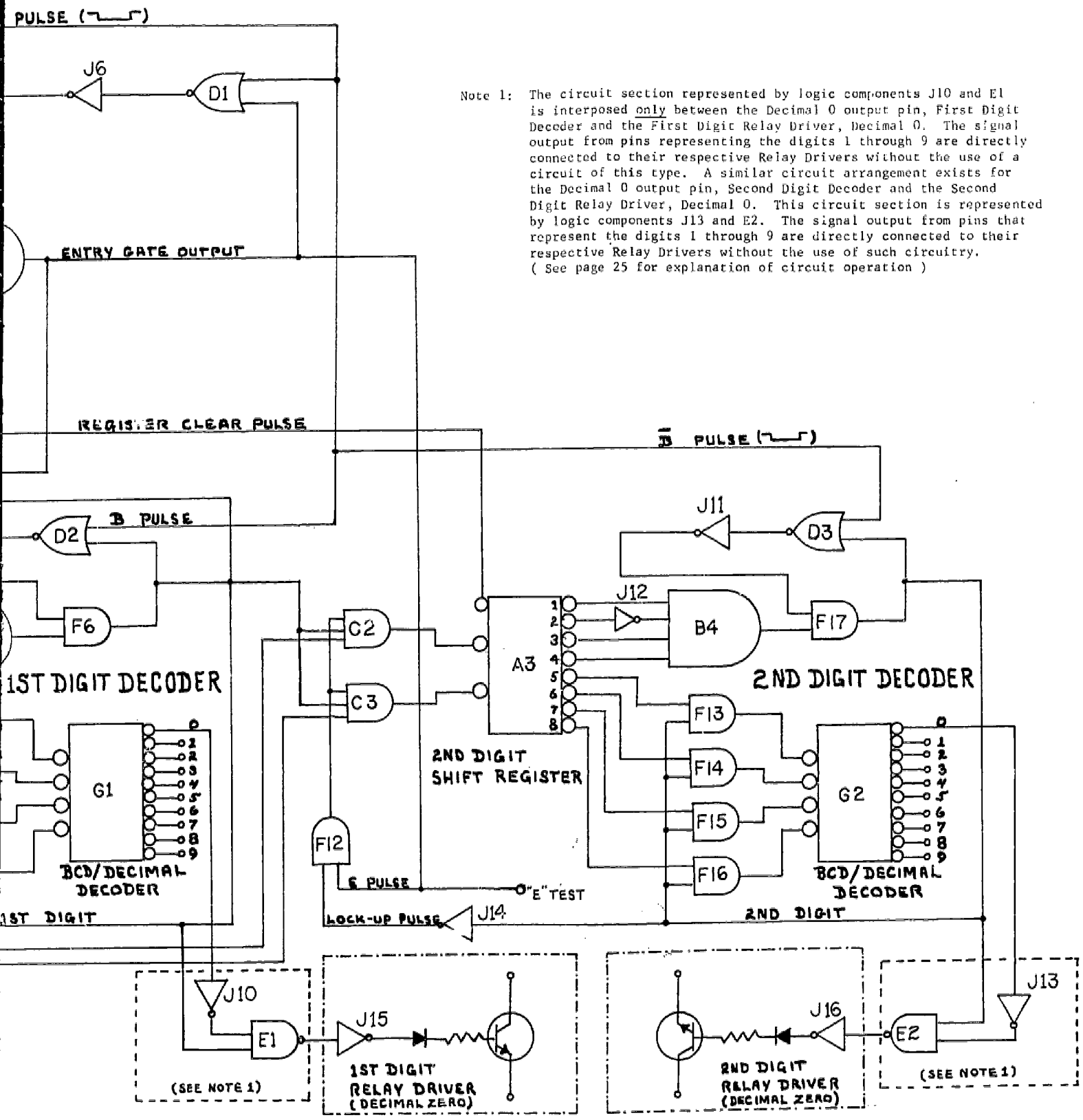
ASCII DECODER - 5 VOLT/16.5 VOLT DC

APPENDIX B

LOGIC DIAGRAMS



LOGIC DIAGRAM - BTL



Note 1: The circuit section represented by logic components J10 and E1 is interposed only between the Decimal 0 output pin, First Digit Decoder and the First Digit Relay Driver, Decimal 0. The signal output from pins representing the digits 1 through 9 are directly connected to their respective Relay Drivers without the use of a circuit of this type. A similar circuit arrangement exists for the Decimal 0 output pin, Second Digit Decoder and the Second Digit Relay Driver, Decimal 0. This circuit section is represented by logic components J13 and E2. The signal output from pins that represent the digits 1 through 9 are directly connected to their respective Relay Drivers without the use of such circuitry.
(See page 25 for explanation of circuit operation)

APPENDIX C

COMPONENT PARTS LIST

Board I - Logic Level Shifter and Synchronization Multivibrators

Number	Type	Description	Manufacturer
1	SN75154N	Quad Line Receiver	Texas Inst.
4	SN74121N	Monostable Multivibrators	Texas Inst.
1	5% Resistor	2K Ω Fixed	--
1	5% Resistor	3K Ω Fixed	--

Board II - Synchronization Multivibrator Timing Components

2	Resistor	5K Ω Variables	--
2	Resistor	10K Ω Variable	--
2	Capacitor	100 uf	
2	Capacitor	50 uf	

Board IIa - Activation Relay and Driver, Activation and Clear Multivibrators/ Timing Circuits

3	SN74121N	Monostable Multivibrators	Texas Inst.
2	Resistors	10K Ω Variable	--
2	Resistors	10K Ω Fixed	--
2	Capacitors	50 uf	--
3	1N4001	Diode	Texas Inst.
1	Resistor	4.7K	--
1	2N3704	Power Transistor	Texas Inst.

Board III - Control Gate Decoder

Number	Type	Description	Manufacturer
2	SN7408N	Quad 2-input AND	Texas Inst.
2	SN7496N	5-bit bi-stable Latch	" "
2	SN74H21N	4-input AND	" "
1	SN74H11N	3-input AND	" "
2	SN7404N	Hex Inverter	" "
1	SN7402N	Quad 2-input positive NOR	" "

Board IV - Ist Digit (Level I) Decoder

3	SN7408N	Quad 2-input AND	Texas Inst.
2	SN7496N	5-bit bi-stable Latch	" "
1	SN74H21N	Dual 4-input AND	" "
3	SN7404N	Hex Inverter	" "
1	SN7442N	BCD-to-Decimal Decoder	" "
1	SN7400N	Quad 2-input Positive NAND	" "
1	SN7402N	Quad 2-input Positive NOR	

Board V - 2nd Digit (Level II) Decoder

3	SN7408N	Quad 2-input AND	Texas Inst.
2	SN7496N	5-bit bi-stable Latch	" "
1	SN74H21N	Dual 4-input AND	" "
1	SN74H11N	Dual 3-input AND	" "
3	SN7404N	Nex Inverter	" "
1	SN7442N	BCD-to-Decimal Decoder	" "
1	SN7400N	Quad 2-input positive NAND	" "
1	SN7402N	Quad 2-input positive NOR	" "

Boards VI and VII

Number	Type	Description	Manufacturer
6	SN7404N	Hex Inverter	Texas Inst.
61	1N4001	Diode	" "
20	5% Resistor	4.7K Ω	" "
20	2N3704	NPN Power Transistor	" "
20	Relay, Miniature	MV7217	Elgin
Power Supply - 5-Volts Regulated (2 each)			Texas Inst.
2	1N4002	Diode	
1	TIP31A	Power Transistor	" "
1	2N5449	Transistor	" "
1	2N4059	Transistor	" "
1	1N746A	Diode	" "
1	3.3 Kohm	Resistor (5%)	
1	1500 ohm	Resistor (5%)	
1	820 ohm	Resistor (5%)	
1	1 Kohm	Resistor (variable)	
1	3.9 Kohm	Resistor (5%)	
3	250uf/25 volt	Filter Capacitor	

Power Supply - 16 Volts Regulated

Number	Type	Description	Manufacturer
2	1N4004	Diode	Texas Inst.
1	TIP31A	Power Transistor	Texas Inst.
1	2N5449	Transistor	Texas Inst.
1	2N4059	Transistor	Texas Inst.
1	1N746A	Diode	Texas Inst.
1	19.5 Kohm	Resistor (10%)	
1	6.8 Kohm	Resistor (10%)	
1	47 Kohm	Resistor (10%)	
1	1000 ohm	Resistor (10%)	
2	-200 uf	Capacitor	

Miscellaneous Parts:

2	F-41X	115 Volt Primary/25.2 Volt Secondary Center Tapped Filament Transformer	TRIAD (Litton Inds.)
1	KB17D	Latching Relay 24 Volt coils	Potter and Brumfield
1		Switch DPDT 115 Volt/ 5.0 Amp	--
1		Light & Socket 24 Volt	--
1	17-20370	Plug body (Male) 37 Contact	Amphenol
1	17-10370	Plug body (Female) 37 Contact	Amphenol
2	17-313-01	Strain Release	"
25	220-P01	Wire Form Contacts (Male)	"
25	220-S01	Wire Form Contacts (Female)	"

Miscellaneous Parts (Cont.)

Number	Type	Description	Manufacturer
1	222-11 N31	Plug Body (Male)	Amphenol
1	222-22 N31	Plug Body (Female)	"
1	222 519	Strain Release	"
25	220-P02	Relia-Tac Contacts (Male)	"
25	220-S02	Relia-Tac Contacts (Female)	"
20 Feet	8459	Cable - 25 Strand insulated	Belden
1	14"x14"x7"	Enclosure	--

Selection Matrix Numeric Call to Select a Given Slide with ASCII Decoder/RA 950

Slide No.	High Order (Level I)	Low Order (Level II)	Slide No.	High Order (Level I)	Low Order (Level II)
0	0	0	41	4	5
1	0	1	42	4	6
2	0	2	43	4	7
3	0	3	44	4	8
4	0	4	45	5	0
5	0	5	46	5	1
6	0	6	47	5	2
7	0	7	48	5	3
8	0	8	49	5	4
9	1	0	50	5	5
10	1	1	51	5	6
11	1	2	52	5	7
12	1	3	53	5	8
13	1	4	54	6	0
14	1	5	55	6	1
15	1	6	56	6	2
16	1	7	57	6	3
17	1	8	58	6	4
18	2	0	59	6	5
19	2	1	60	6	6
20	2	2	61	6	7
21	2	3	62	6	8
22	2	4	63	7	0
23	2	5	64	7	1
24	2	6	65	7	2
25	2	7	66	7	3
26	2	8	67	7	4
27	3	0	68	7	5
28	3	1	69	7	6
29	3	2	70	7	7
30	3	3	71	7	8
31	3	4	72	8	0
32	3	5	73	8	1
33	3	6	74	8	2
34	3	7	75	8	3
35	3	8	76	8	4
36	4	0	77	8	5
37	4	1	78	8	6
38	4	2	79	8	7
39	4	3	80	8	8
40	4	4			

ASCII Decoder to RA 950 Projector Cable Wiring Code
(Pin Numbering Coincides with RA-950 Sehcmatic, Appendix A)

Pin No.	Function	Color Code
1	Low order Digit 5	White-red
2	Low order Digit 2	White-black
3	Low order Digit 8	Green-white
4	Low order Digit 3	Green
5	Not used	Red-black
6	Low order Digit 6	Blue-black
7	Low order Digit 1	Orange
8	Low order Digit 7	Blue-red
9	Low order Digit 9	Red-white
10	High order Digit 3	Red
11	Low order signal voltage feedback	Blue-white
12	High order Digit 6	Black
13	High order Digit 4	White
14	High order Digit 1	Blue
15	High order Digit 7	Orange-black
16	High order Digit 5	Black-white
17	High order Digit 2	Red-black-white
18	High order Digit 8	Orange-red
19	Projector ON/OFF voltage	Green-white-black
20	Low order Digit 0	Orange-green
21	High order Digit 0	Red-green
22	Cycle voltage	Green-black
23	Not used	Black-red-white
24	Cycle voltage return	Black-red
25	Projector ON/OFF voltage return	White-black-red

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